IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shui-Ming Cheng, et al.	?	Group Art Unit: 2814
Serial No.: 10/722,218	?	Examiner: Cao, Phat X.
Filed: November 25, 2003	?	
For: Semiconductor Device Having High Drive Current and Method of Manufacture Therefor	§	Confirmation No.: 6790

Mail Stop RCE
Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. ? 1.131

I, Yi-Ming Sheu, declare and say that:

1. I am one of the four sole inventors of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was an employee of Taiwan Semiconductor Manufacturing Co., Ltd., the assignee of the above identified application (hereinafter referred to as SMC? , in Taiwan.

3. The invention claimed in the above-identified application was reduced to practice prior to August 12, 2003, the filing date of U.S. Patent App. No. 10/639,170, which is the parent application of divisional U.S. Patent App. No. 11/407,633, as evidenced by the TSMC Invention Disclosure form that I approved before August 12, 2003. A redacted copy of the TSMC Invention Disclosure form is attached.

4. All of the activities described above occurred in Taiwan.

Appl. No. 10/722,218
Declaration under 37 C.F.R. ? .131

Patent/Docket No. 24061.149
Customer No. 000042717

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

✓ Yi-Ming Sheu

Yi-Ming Sheu

Date: ✓ Aug-06-2007

tsmc TSMC INVENTION DISCLOSURE

SECURITY & TSMC RESTRICTED

SMCHENGA/TSMC on [redacted] 09:38:34 AM

Status : 待智財處處理 24061.149 Current Processer : 005728 : 謝淑惠

HB

Disclosure No.	TSMC0[redacted]-0959	Received date	[redacted]	Process priority	

Emp. No. (for the inventors from outside of tsmc, please use "x66" instead)	Full name of inventor(s) English, the same as passports	Chinese	Dept.	Dept. Code	Ext. No.	E-mail Address
025302	Shui-Ming Cheng	鄭水明	ADTD	2362	712-5125	SMCHENGA@tsmc.com.tw
024734	Ka-Hing Fung	馮家馨	ADTD	2362	712-5190	KHFUNG@tsmc.com.tw
025246	Kuan-Lun Cheng	程冠倫	ADTD	2362	712-5128	KLCHENG@tsmc.com.tw
007519	Yi-Ming Sheu	許義明	ADTD	2362	712-5836	YMSHEU@tsmc.com.tw

- Title of invention – (English only)
  Method of manufacturing the semiconductor device with high drive current
- Related disclosure(s) –
- Assignee – 本發明屬於1.TSMC 或 2.由TSMC與其他公司共同擁有
  ● 1. TSMC ○ 2. TSMC &
- Laboratory Notebook / 研究紀錄簿相關資訊

  This idea was shown on page of the laboratory notebook with serial number of (such as 2002-00036).

  Please attach a copy of the related pages.
- Invention related information / 本發明相關資訊 –

  1. Will this invention be disclosed, published, utilized, commercialized or implemented in Customer's product(s)?
  ● No. ○ Yes. When (ex. [redacted]) 請務必填寫本發明之預定論文發表或展覽或販賣或實施於客戶產品的日期, 以加速申請流程.

  2. Other special request :

- References similar to the invention / 與本發明相關的論文及/或專利 - (Please search for related patents on USPTO website / www.uspto.gov)

  1. keyword(s) used / 專利查詢所使用的關鍵字 : stressed channel

  2. Related patent number(s) / 相關的專利號碼 : US2003/0080361 A1

  3.Related Non-Patent article(s) and/or product(s) / 其他相關的論文名稱或產品型號 :

- Old method(s) or product(s) for performing the purpose of this invention / 目前方法簡介 (English only)
  device with stressed channel can improve drive current but only favor for NFET or PFET by using CESL and S/D SiGe epi.

- Problems or disadvantages faced by old method(s) or product(s) / 目前方法所面臨的問題及缺點 (English only)
  high drive current only for NFET or PFET
  can not integrate together by using CESL and S/D SiGe epi

- General purpose of this invention / 發明目的 (English only) -
  Combining CESL and S/D SiGe epi to improve drive current for both NFET and PFET

- Advantages of this invention / 本發明的好處或優點 (English only)
  High drive current
  ease to integrate NFET and PFET

- Points of this invention thought to be novel, list by items. Please identify which elements/steps are must and which elements/steps are optional / 請逐項列舉爲達成發明目的所使用的新方法或手段, 即, 本發明與目前方法的主要不同處, 並請指出必要及非必要元件 (English only)

  dummy nitride spacer to reduce the thermal buget for SiGe epi (if SiGe epi thermal is lower enough, dummy nitride spacer can be deleted)
  recessed S/D to enhance NFET tensile CESL stressed level
  raised S/D to relief PFET tensile CESL stressed level and improve S/D engineering margin

- Detailed description of this invention / 發明的詳細敘述, 至少需包括一最好的實施例, 及/或其他適用於本發明的範例 (English only)
  refer to attached ppt

- Other embodiments/methods/apparatus can be used to achieve the purpose of your invention by a potential infringer./其他可實施本發明目的的手段?或其他可迴避本發明的範例及做法?
  no

- Attachments / 圖形請用附加檔 : patent_High_Ion_procesflow.ppt

-

	SIGNATURE OF WITNESS	DATE	SIGNATURE OF WITNESS	DATE
WITNESS: THE TWO WITNESSES WHOSE SIGNATURES APPEAR BELOW HAVE READ AND UNDERSTOOD THIS ENTIRE INVENTION DISCLOSURE.	王易妤	[redacted]	姚舒涵	[redacted]

DISCLOSURE SUBMITTED BY			
INVENTORS' EMPNO	INVENTORS' NAME	INVENTOR'S SIGNATURE	DATE

025302	鄭水明	鄭水明 馮家馨 程冠倫 許義明	[redacted]
024734	馮家馨		
025246	程冠倫		
007519	許義明		

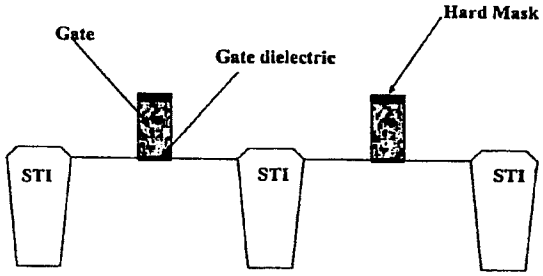
Processing Log :

Motivation

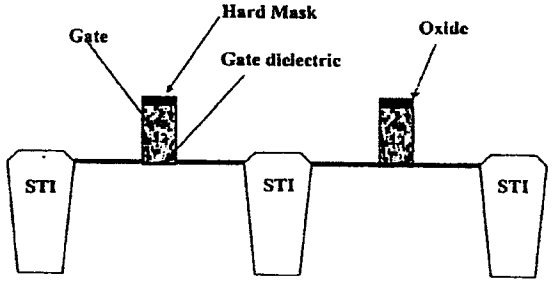
- From the literatures, we know that the tensile and compressive CESL will improve drain current for nFET and pFET, respectively. But it is hard to integrate both tensile and compressive CESL into CMOS technology.Even for S/D-SiGe method only improves pFET drive current.
- So here, we propose a new integrated scheme with high drive current for both nFET and pFET by combining tensile CESL and SiGe.

Key Process Flow (1)

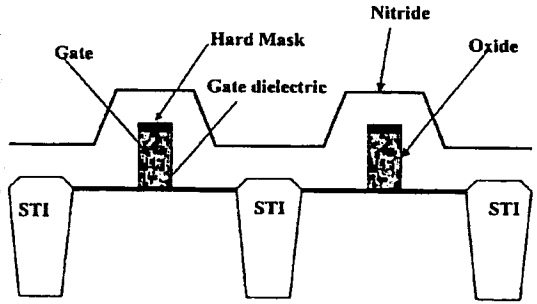
1. Poly Dry Etch



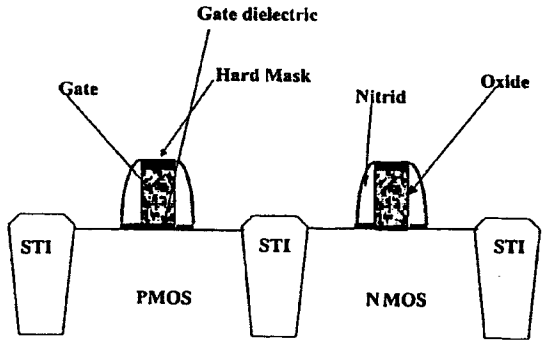
2. Poly Re-oxidation



3. Dummy Nitride Dep.

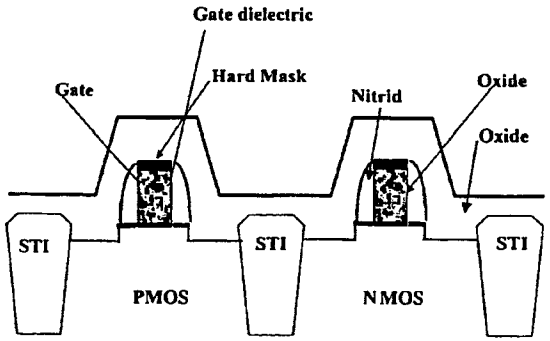


4. Dummy Nitride Etch

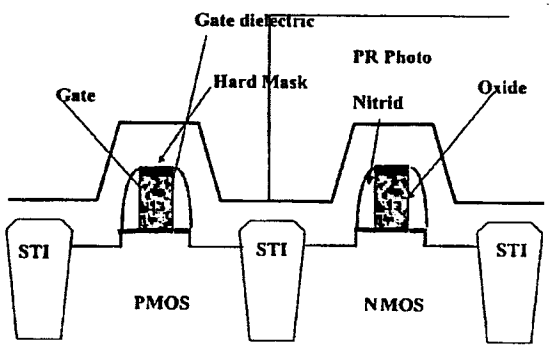


Key Process Flow (1)

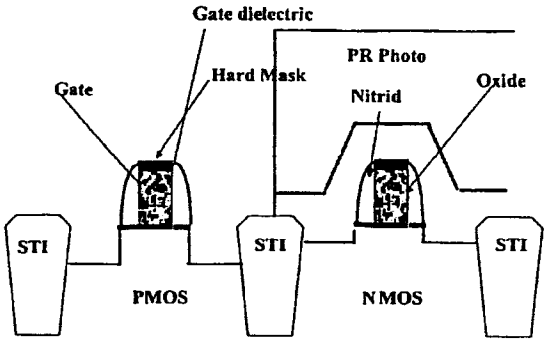
5. S/D Etch
Oxide Dep.



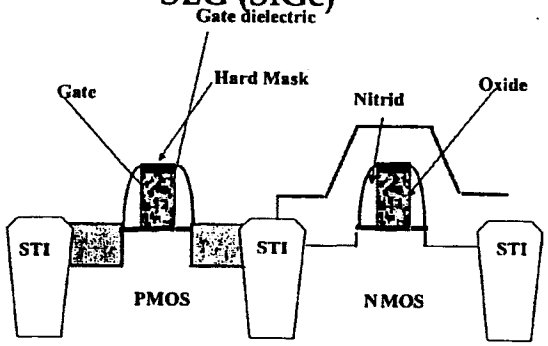
6. NMOS PR Photo
Oxide Remove



7. S/D Etch

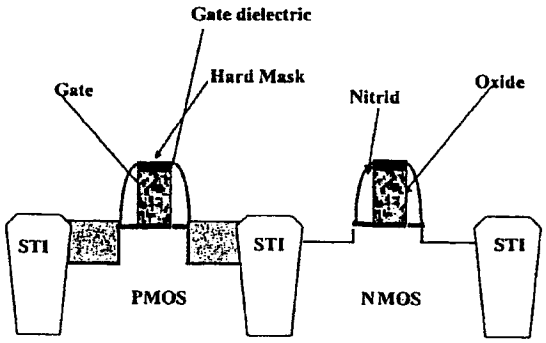


8. NMOS PR Strip
SEG (SiGe)

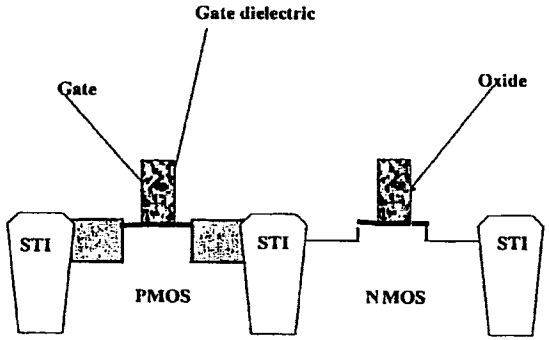


Key Process Flow (1)

9. Oxide remove



10. Nitride/HM Remove



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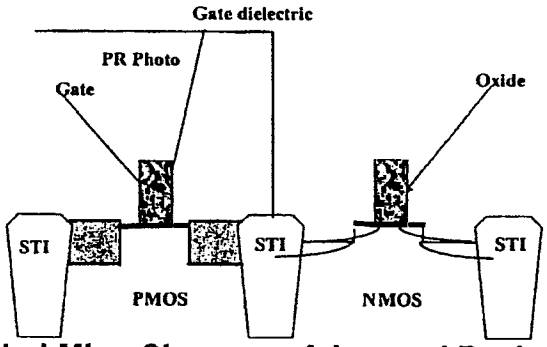
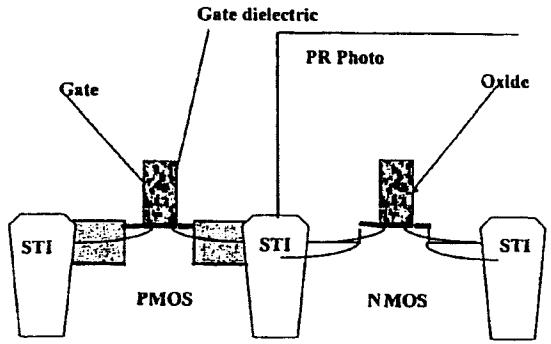
NLDD I/I
PR Strip

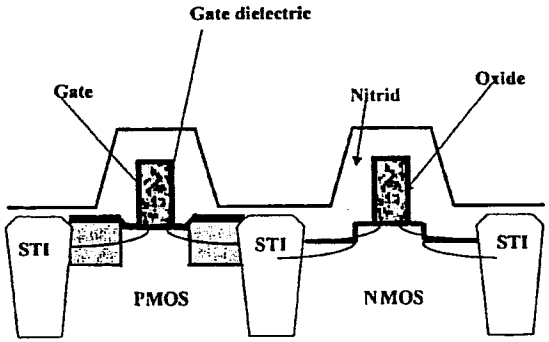


12. NMOS PR Photo
PLDD I/I
PR Strip

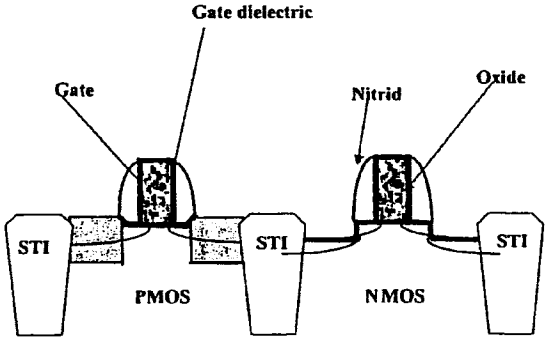


Key Process Flow (1)

12. Liner Oxide Dep.
    Nitride Dep.



13. Nitride Etch



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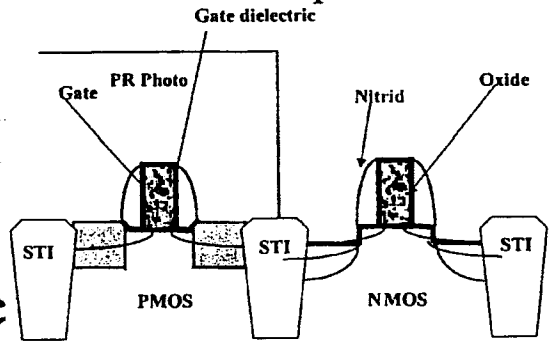
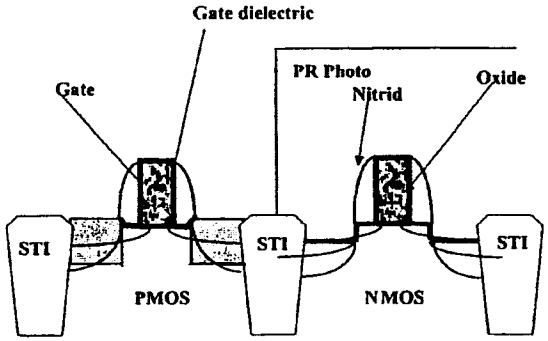
    PR Strip

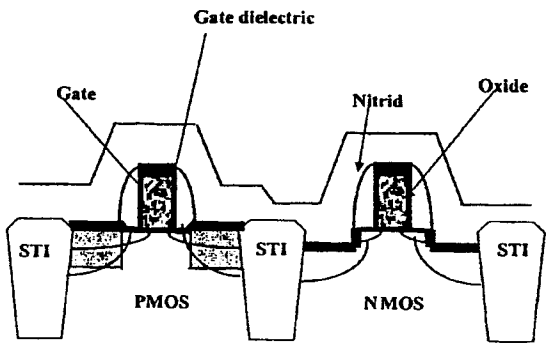


15. NMOS PR Photo
    PSD I/I
    PR Strip



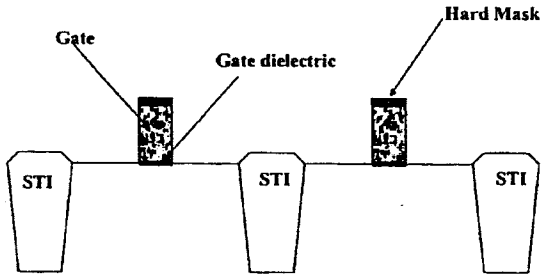
Key Process Flow (1)

16. Salicided
Tensile CESL

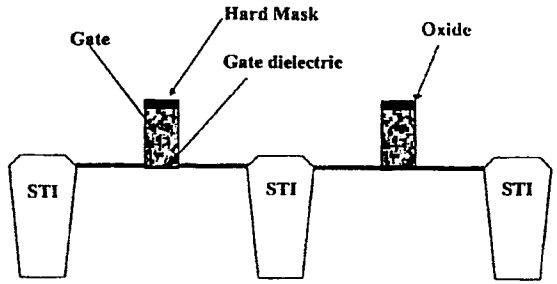


Key Process Flow (2) (If SEG Temp. < 680C)

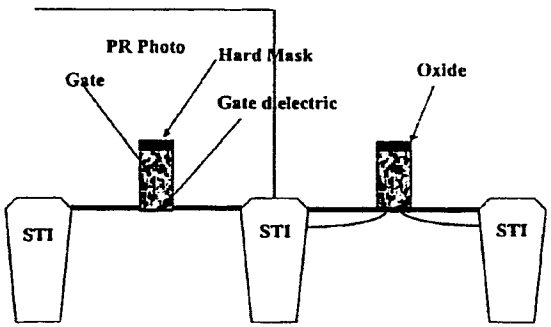
1. Poly Dry Etch



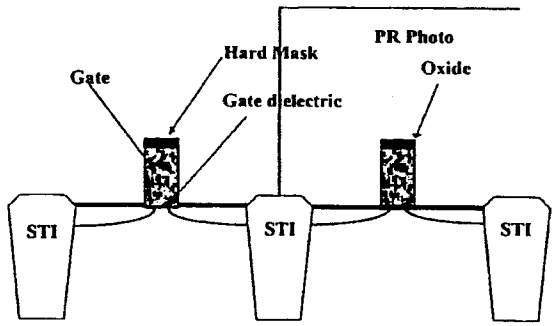
2. Poly Re-oxidation



3. PMOS PR Photo
   NLDD I/I
   PR Strip

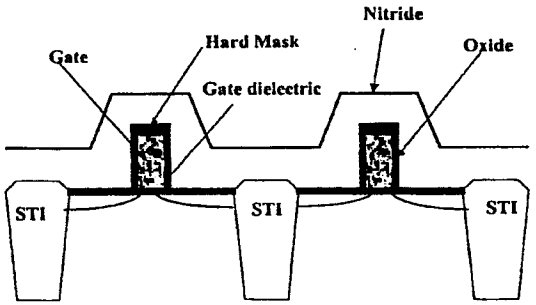


4. NMOS PR Photo
   PLDD I/I
   PR Strip

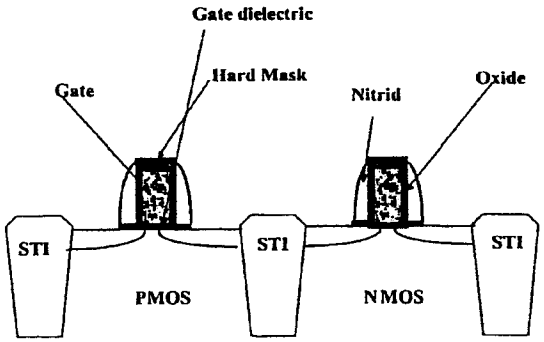


Key Process Flow (2) (If SEG Temp. < 680C)

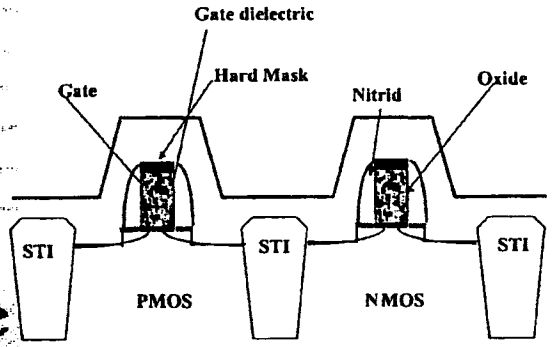
5. Liner oxide Dep.
Nitride Dep.



6. Nitride Etch



7. S/D Etch
Oxide Dep.



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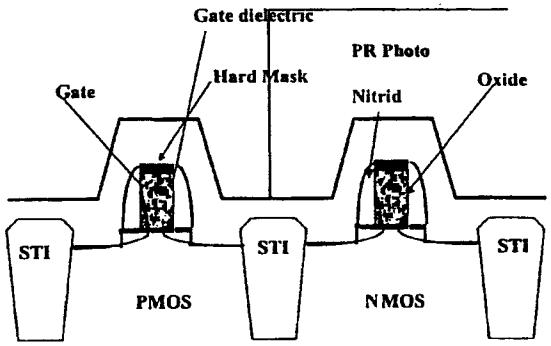
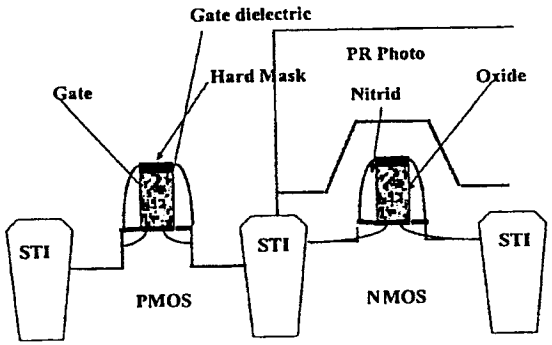
Oxide Remove

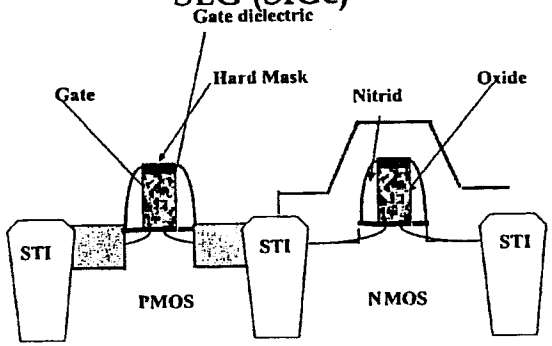


Key Process Flow (2) (If SEG Temp. < 680C)

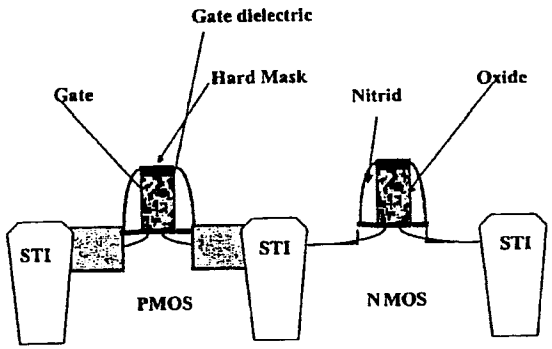
9. S/D Etch



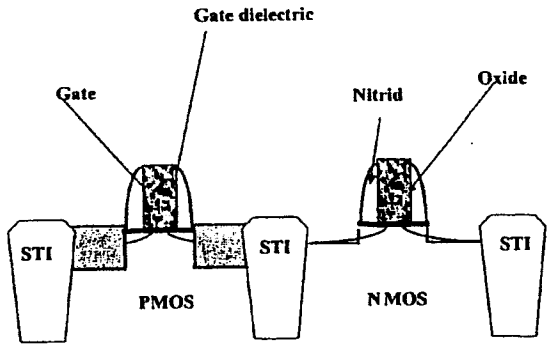
10. NMOS PR Strip
SEG (SiGe)



11. Oxide remove

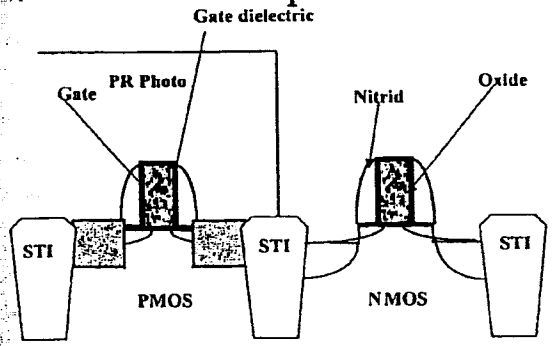


12. HM Remove

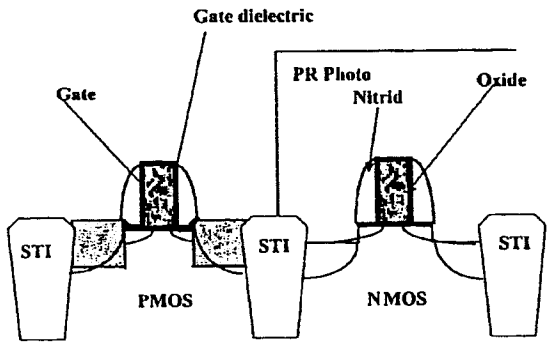


Key Process Flow (2) (If SEG Temp. < 680C)

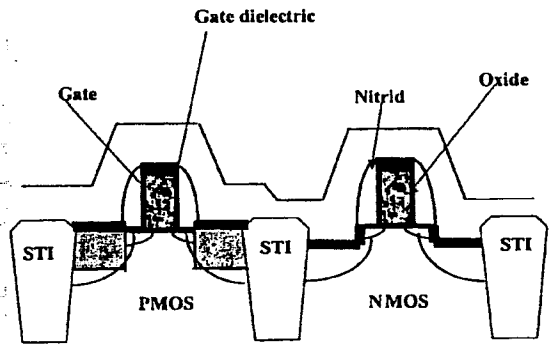
14. PMOS PR Photo
    NSD I/I
    PR Strip



15. NMOS PR Photo
    PSD I/I
    PR Strip



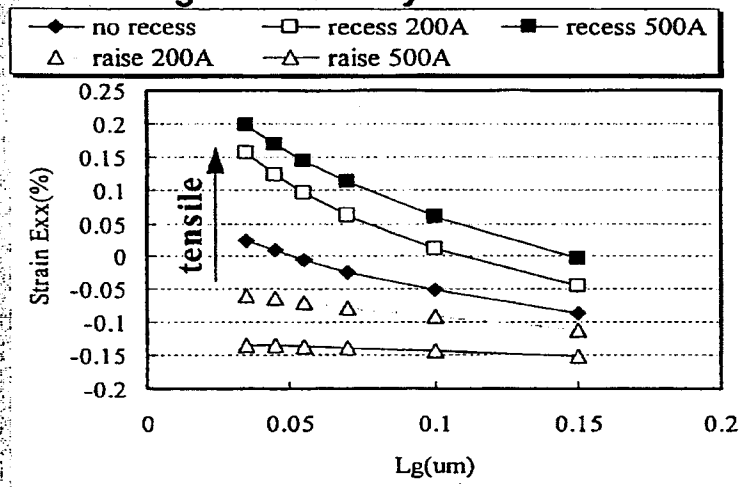
16. Salicided
    Tensile CESL



Stress Enhancement for Recessed/Raised S/D

Cut line 100A below gate oxide

Gate Length Sensitivity



Spacer Width Sensitivity